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**Insulated gate semiconductor device manufacturing method for metal oxide semiconductor field effect transistor, involves annealing silicon semiconductor layer in ultra-high-vacuum or hydrogen atmosphere continuously to form trench**

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002343805	A	20021129	JP 2001141897	A	20010511	200310 B

Priority Applications (No Type Date): JP 2001141897 A 20010511

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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JP 2002343805	A	8	H01L-021/336	
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Abstract (Basic): JP 2002343805 A

**NOVELTY** - A channel layer of reverse conductivity type is formed on a silicon semiconductor substrate that is annealed in ultra-high-vacuum or hydrogen atmosphere continuously to form a trench. A gate insulating film is formed on trench inner wall and surface of channel layer. A gate electrode is formed, under the trench. A source region is formed to adjacent side of the trench.

**USE** - For manufacturing insulated gate type semiconductor device for e.g. metal oxide semiconductor field effect transistor (MOSFET) used in mobile telephone, personal digital assistant, etc.

**ADVANTAGE** - MOSFET has high reliability, and improved cell density with reduced resistance. Short circuit between the gate and source is suppressed.

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Title Terms: INSULATE; GATE; SEMICONDUCTOR; DEVICE; MANUFACTURE; METHOD; METAL; OXIDE; SEMICONDUCTOR; FIELD; EFFECT; TRANSISTOR; ANNEAL; SILICON; SEMICONDUCTOR; LAYER; ULTRA; HIGH; VACUUM; HYDROGEN; ATMOSPHERE; CONTINUOUS; FORM; TRENCH

Derwent Class: L03; T01; U11; U12; W01

International Patent Class (Main): H01L-021/336

International Patent Class (Additional): H01L-029/78

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C11C1; L04-C12; L04-C16A; L04-E01B1

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